

Evolution of a Flexible Architecture for 802.11a/b Radios



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System Architecture Tradeoffs

Superheterodyne vs. Direct Conversion

- Superhet is a proven architecture but requires additional down-conversion and filtering
- Direct conversion has problems with DC offset, LO Leakage and $1/f$ noise

I/Q vs. IF Sampling

- I/Q Sampling Allows for Image Reject Mixing
 - Also requires $1/2$ the sampling rate
 - Must control I/Q Imbalance to tight tolerances
- IF Sampling eliminates I/Q Imbalance issue at the expense of higher sampling rate
 - Also requires greater dynamic range (#bits) in A/D

Key Component Limitations

SAW Filter

- Provides first protection against next adjacent channel
- Limited to ~465MHz max with reasonable rejection and insertion loss

A/D Converter

- ASIC based converters were limited to 40 MHz sample rates at 10bits
- Also limited in RF Bandwidth to ~ 100MHz, 200MHz is desired

Crystal Oscillator

- Spec requires ≤ 20 ppm jitter
- Performance gets tougher with increasing frequency
- Maximum frequency at low cost was 20MHz

Transmit Filters

- Filter pass band of 5170 - 5330MHz
- LO rejection need 60dB of rejection 315MHz from band edge
- No good filters available from suppliers
 - Best was a 1" x 3" filter which cost \$8 in 500K qty

IF Frequency Plan

Front end for lower UNII bands is 200MHz;

5.15 - 5.35GHz

IF Frequency Selection Limited by SAW Filter

- **Desire an IF \gg 200MHz to allow filtering of out of band components**

UNII Band Channels on 5MHz Boundaries

Systemonic Design Uses a 465MHz IF

Baseband Interface

Waveform Requires Sample Rate = $n \cdot 20\text{MHz}$

- 64 Samples per 3.2 microsecond period

80 MHz Sample Rate Allows for Digital Downconversion

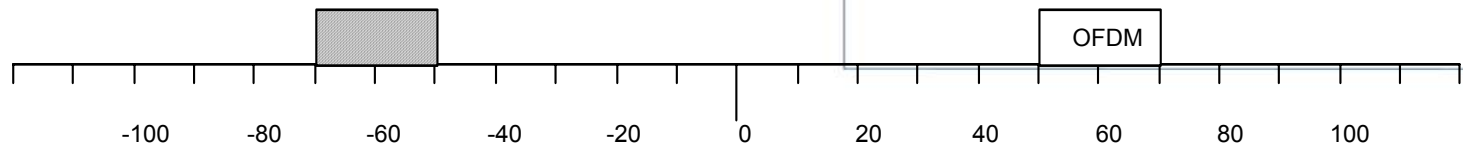
- Hilbert Transform requires only simple $\pm 1, 0$ operations
- Can down-convert, decimate and filter in one operation

Normal Choices are 20MHz and 60MHz (Image of -20MHz)

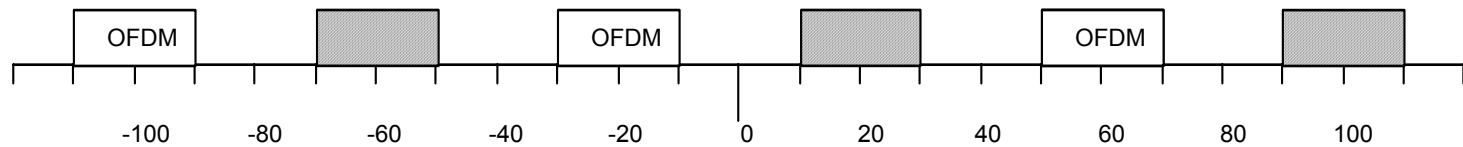
60MHz Selected to simplify baseband filtering

Sampling Frequency Diagram

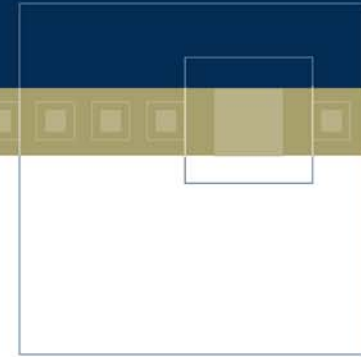
IF Frequency = 60 MHz



$F_s = 80 \text{ MHz}$



Crystal Oscillator Tradeoff



Oscillator Requirements

- Jitter < 20ppm
- All clocks must be derived from the same sources

Crystal

- Standard crystal sources provide 20-25ppm at reasonable cost
- Performance is worse for frequencies > 20MHz
 - Typical cost in high volume of less than \$1
- TCXO's provide an order of magnitude improvement at additional cost
 - Typical cost in high volume of \$2.73

Phase Noise Requirements

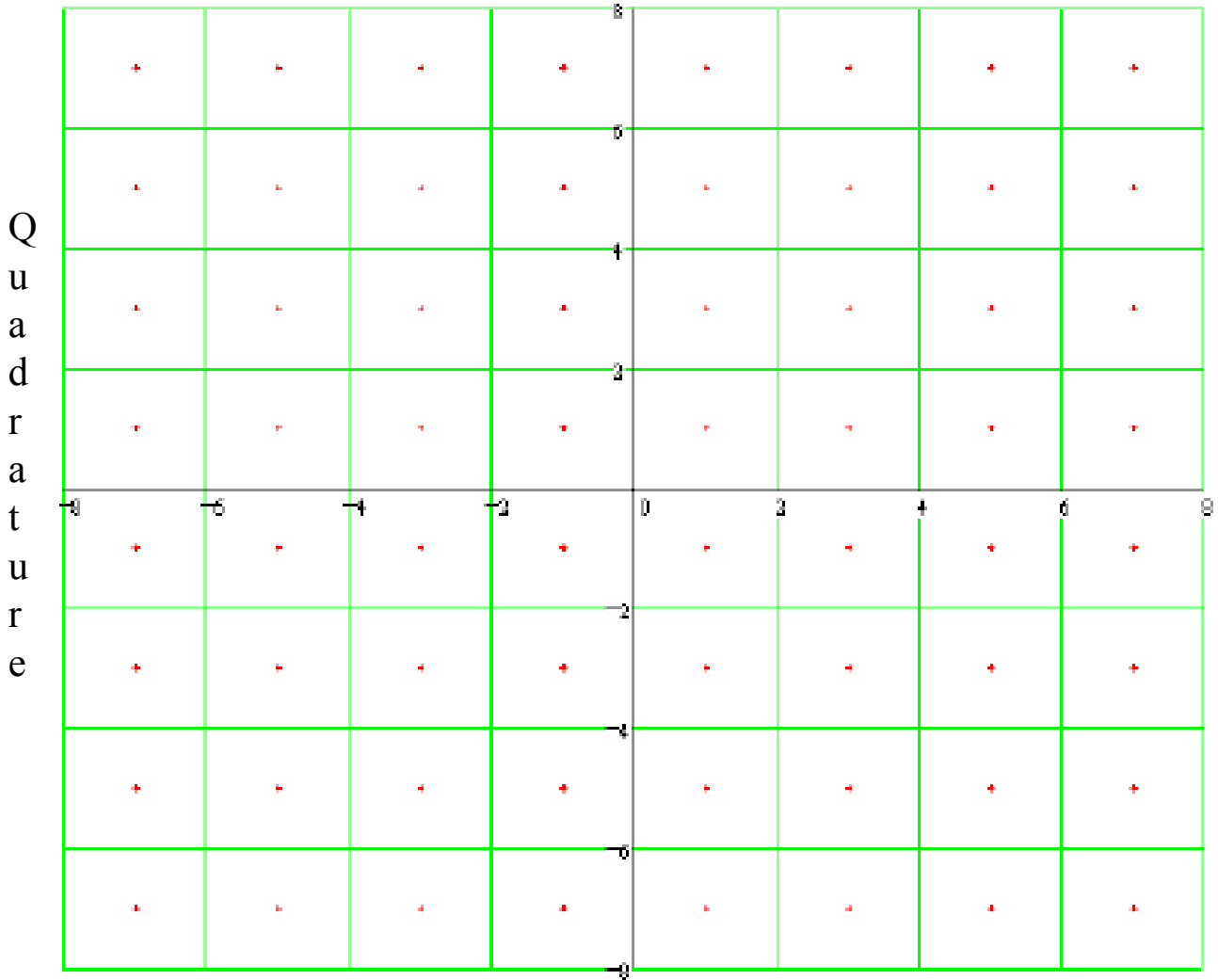
High Order QAM Waveforms Require Better Linearity and Lower Phase Noise to Achieve a Good BER

- -38dBc integrated phase noise yields $\sim 1^\circ$ Error
 - Corresponds to ~ 0.5 dB C/N loss (64QAM, 10^{-5} BER)

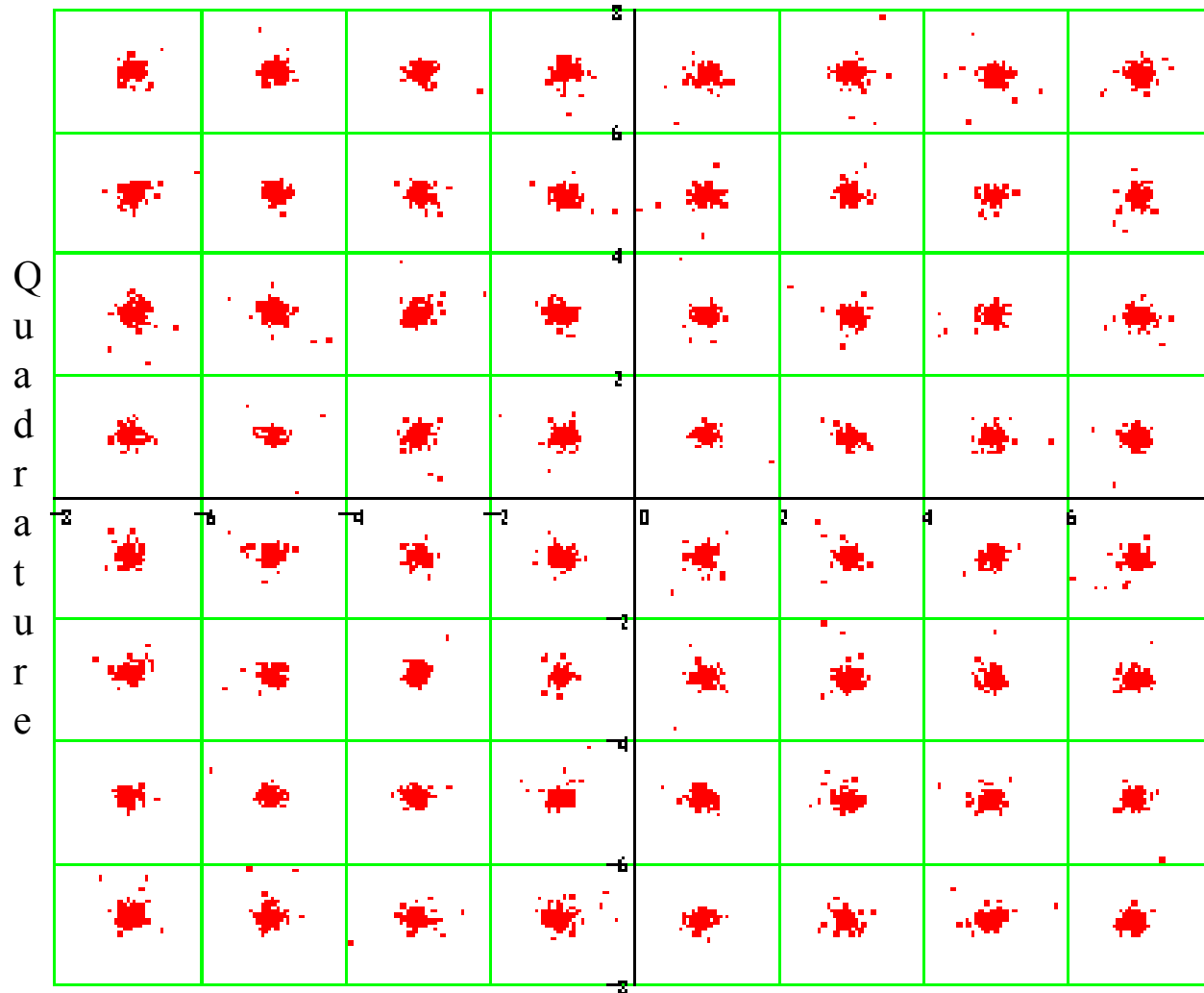
Phase Noise Can Not be Predicted or Compensated

A Major Contributor to System Phase Noise is the VCO

64 QAM Modulation (Ideal)



64 QAM Modulation (w/ Noise)



Off chip VCO provides most flexibility but requires additional components over a highly integrated solution

- **VCO can be built with low phase noise**
- **Offers low risk approach with option for alternate components**

On chip VCO's offer the potential for lower system cost but are limited by the semiconductor process selected

- **One of the highest risk areas for chip development**
- **Limits applications to the frequency plan selected**

SiGe vs. CMOS

System Requirements

- Constellation Accuracy is Driven by Phase, Amplitude Error
- Using IF Sampling (Not I/Q) Lets Synthesizer Use Majority of Error Budget

Existing Synthesizer

- Off Chip VCO, PLL, Loop Filter Network
- -37.5dBc Integrated Phase Noise (Equivalent to 1.09° of Error)
 - BER (64QAM) = 10^{-5} for a CNR = 25dB

State of the Art CMOS Synthesizer (Paper by Rategh, et. Al.)

- Integrated on Chip
- -21.4dBc Integrated Phase Noise (Equivalent to 6.87° of Error)
 - BER (64QAM) = .05 for a CNR = 25dB (PER = 100%)

System Impact and Tradeoffs:

- CMOS VCO's Can Cause a Tremendous Increase in Bit Error Rate (BER)
- Off Chip Components Cost More (\$5.65 for Dual PLL and 2 VCO's)
- High Performance VCO's & PLL's Allow Relaxing Other Component Specs

Flicker Noise (1/f Noise) is a Greater Problem for CMOS Devices

- Tends to be modulated onto the RF signal
- Flicker noise sees high conversion gain in mixers with a baseband output,
- Main way to reduce it in MOS devices is to increase the transistor's size
 - Decreases RF Gain
 - Increased die size and power dissipation

Power Handling and Scaling

- Analog CMOS devices do not scale with geometry
- SiGe devices higher f_T requires less gain stages, power for given P1dB

Tondelayo™ RF & IF Chips Are Fabricated With SiGe

RF Switch Tradeoffs

Switches Are Required for T/R and Antenna Diversity Selection

5GHz Switches Have Typical Insertion Loss of 1.5 - 2.0dB

- **Combined insertion loss of 3 - 4 dB**
- **Loss contributes to receive noise figure and power dissipation**

Low Loss Switches are Realizable in GaAs but Require a Negative Voltage Supply

- **Tondelayo™ PA/Switch provides a combined insertion loss of 1.5dB for two 5GHz switches**

Power Supply Tradeoffs

Standard PCI / Cardbus Supply Voltage is 3.3VDC +/-10%

Desire Separately Regulated Supplies for Analog Circuitry

- Require low noise supplies to meet performance and regulatory specification
- Digital circuits generate lots of broadband switching noise

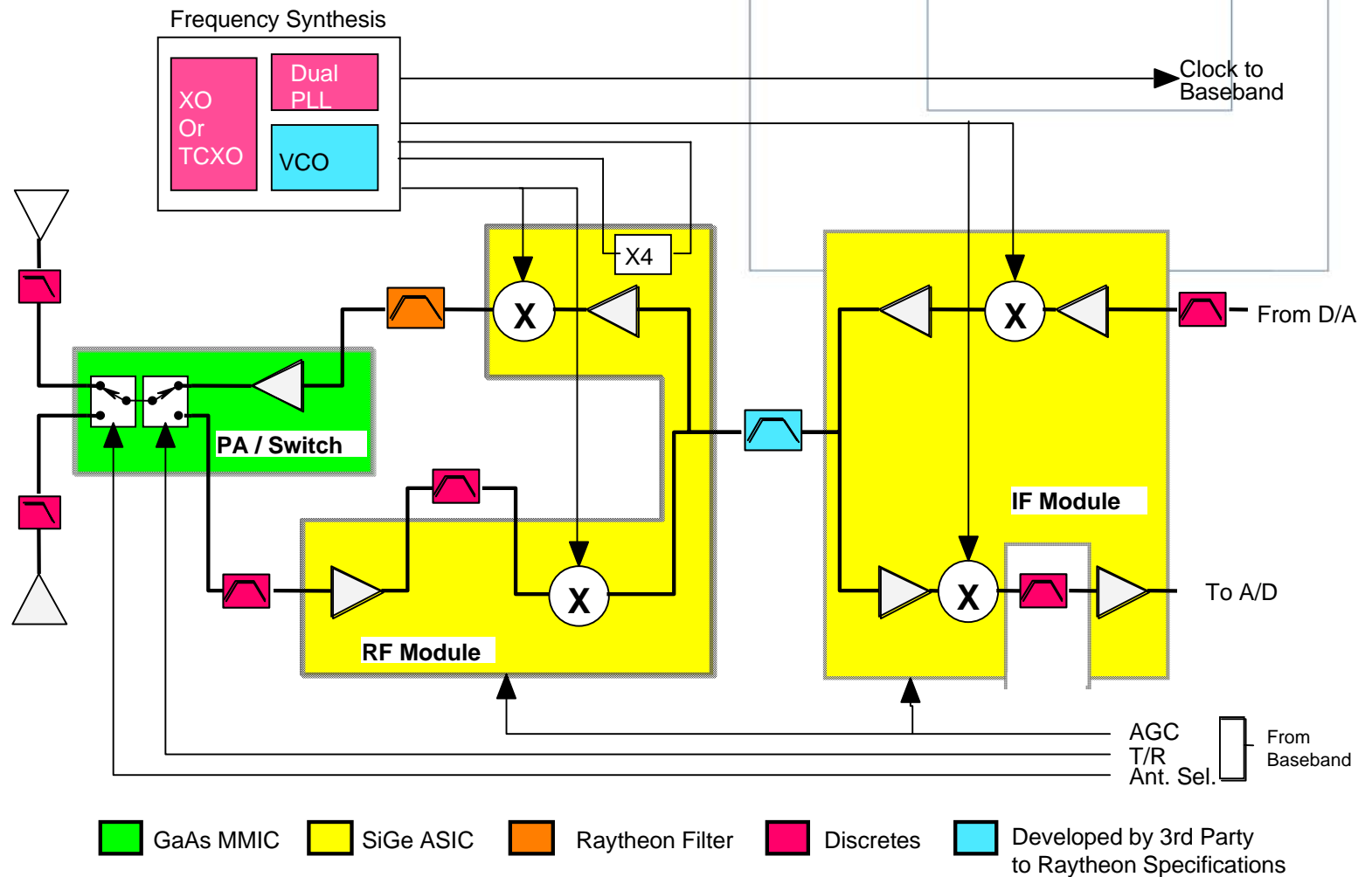
Two Leading Options

- Design the analog components and circuitry to work at 3.0VDC (nominal)
- Boost up, then regulate down to 3.3VDC (traditional)

We Chose 3.0VDC to Minimize Overall System Cost

- Requires more care and ingenuity in the design of the chips

Analog Subsystem Diagram



DSP vs. Dedicated Hardware

DSP Advantages

- **Flexibility**
 - DSPs move implementation into software
 - Re-usability of DSPs is higher than dedicated ASICs
- **Upgrade capability**
 - Evolution of algorithms possible
 - Ability to upgrade, track, and follow standards
- **Time to market**
 - Parallel validation of hardware and algorithms possible
- **Reduction of Design Risk**
 - Algorithms are often validated in the field
 - Later algorithm fixes are possible

Traditional Hardware Advantages

- **More efficient use of real estate (die area) = lower cost**
- **Lower Power**

Systemonic's DSP Based Approach

Apply Flexibility (Programmability) Where it is Required

Tailor the Programmable Platform to the Applications Needs

- Processing power (datapath parallelism, SIMD)
- Instruction set architecture (ISA)
- I/O, peripherals and memory subsystem

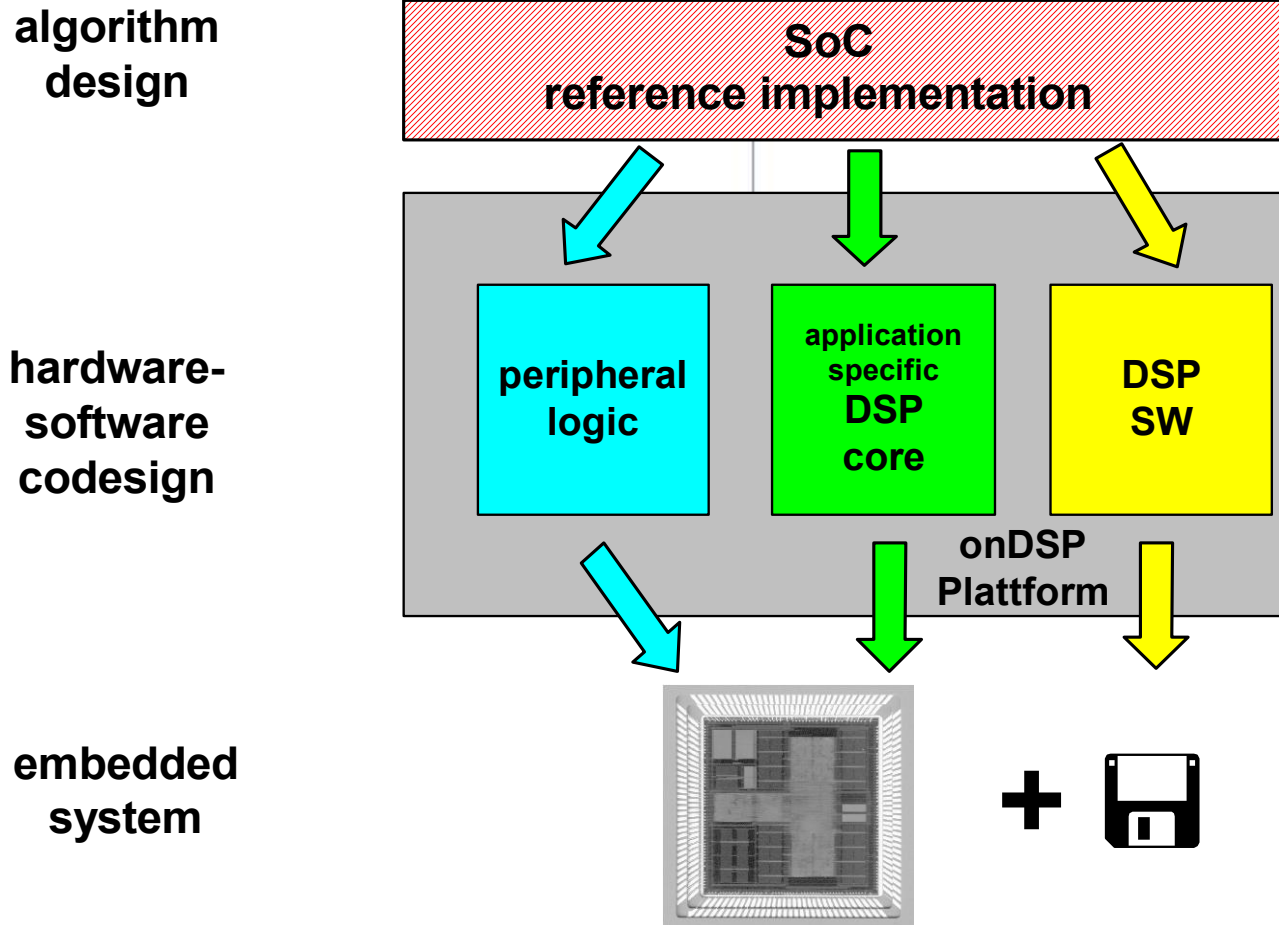
Design From a Common Architecture Data Base

- Highly automated generation of tailored derivatives
- Generation of SW development tools from same data base

DSP Architecture

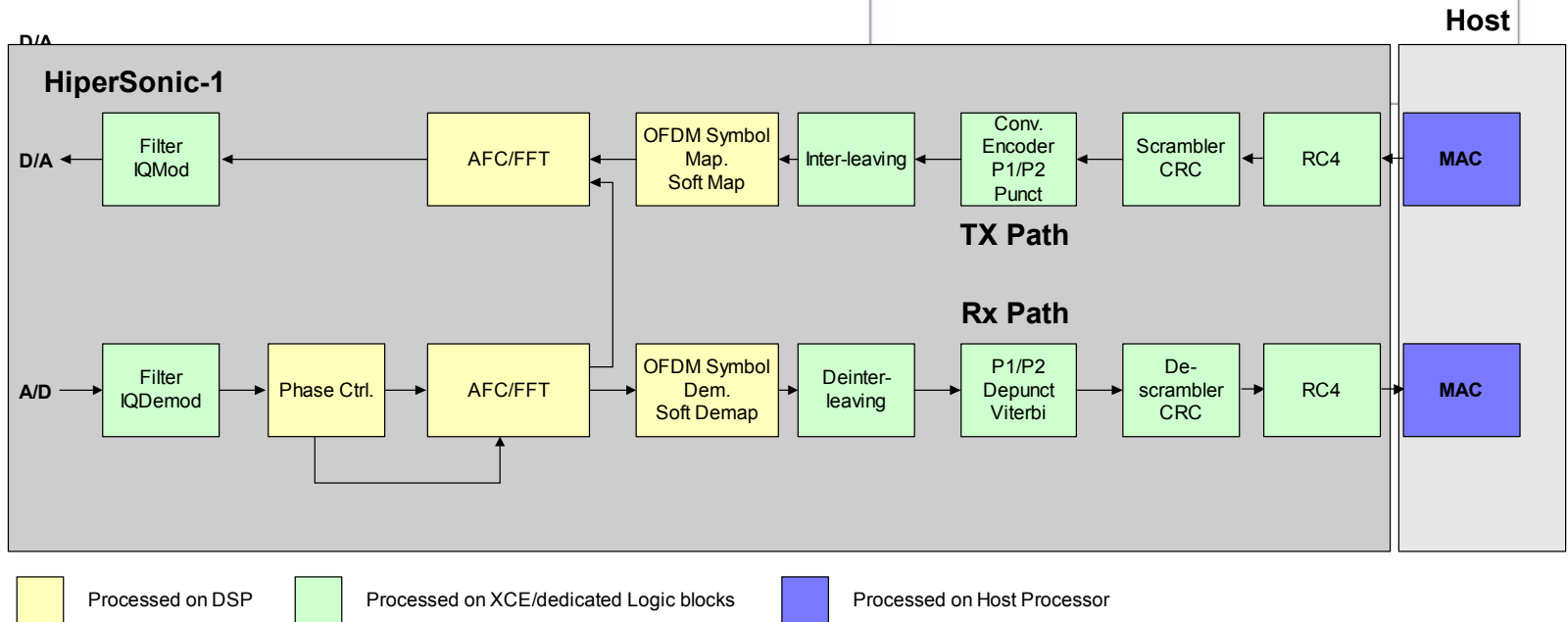
- SIMD mode + flexible datapath interface
 - Optimized in conjunction with algorithm design
- SISD mode 32 bit RISC, 16/32 bit DSP
 - Allows compiler/programmer friendly programming

DSP Based Design Process



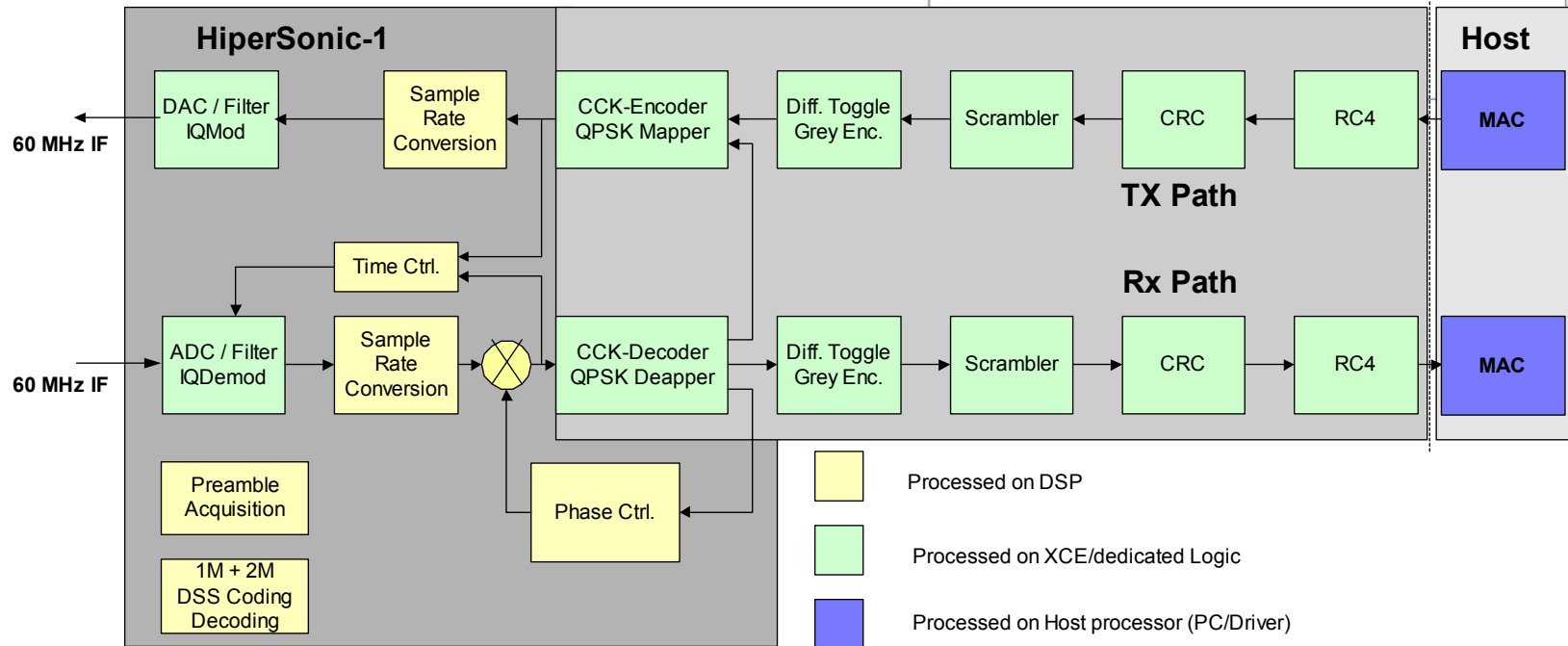
802.11a Algorithmic Partitioning

802.11a Burst Encoding / Decoding Algorithmic Partitioning on Tondelayo-1



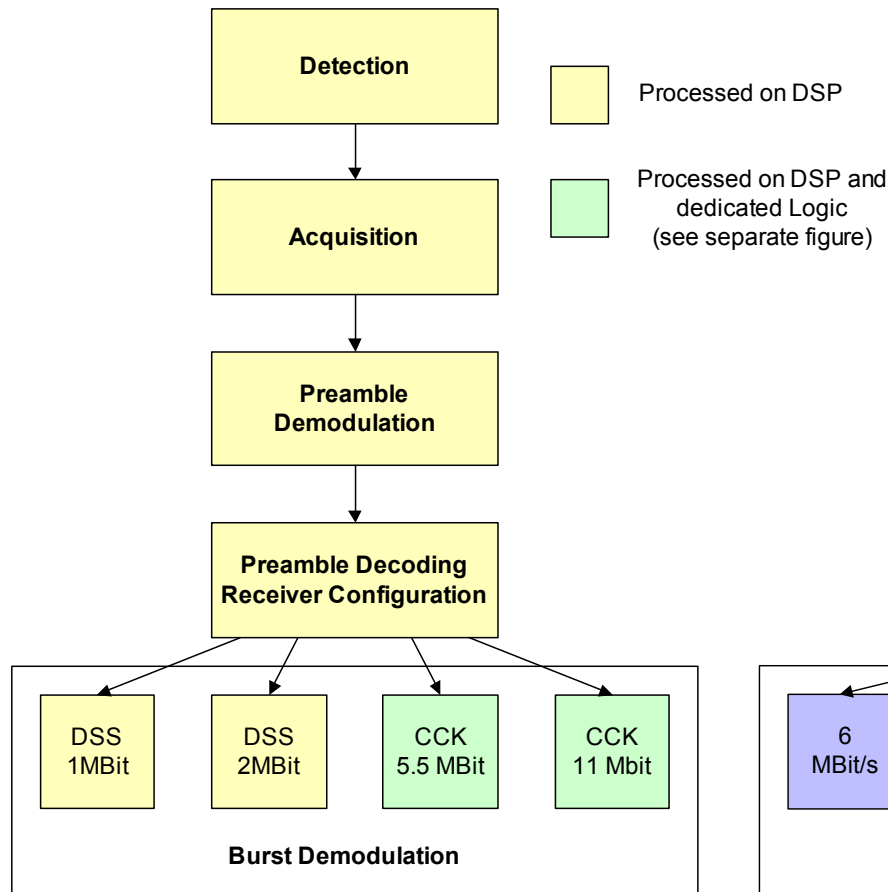
802.11b Algorithmic Partitioning

802.11b Burst Encoding / Decoding Algorithmic Partitioning on Tondelayo-1

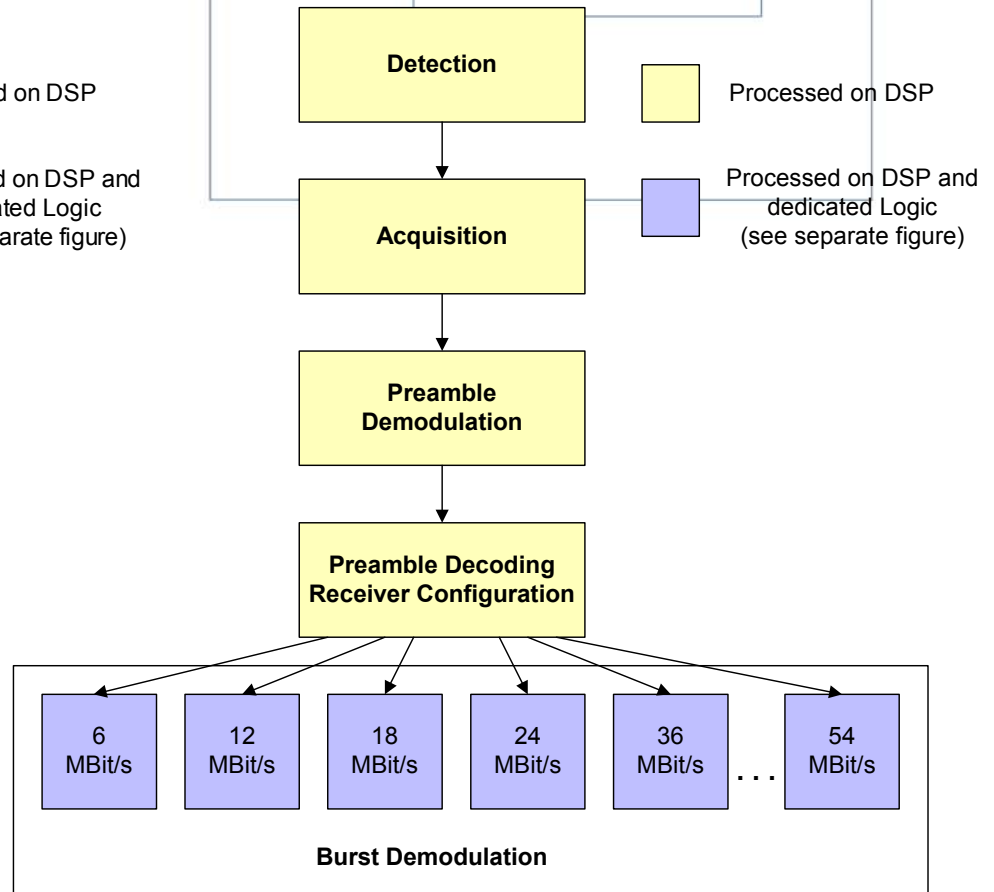


Acquisition Processing

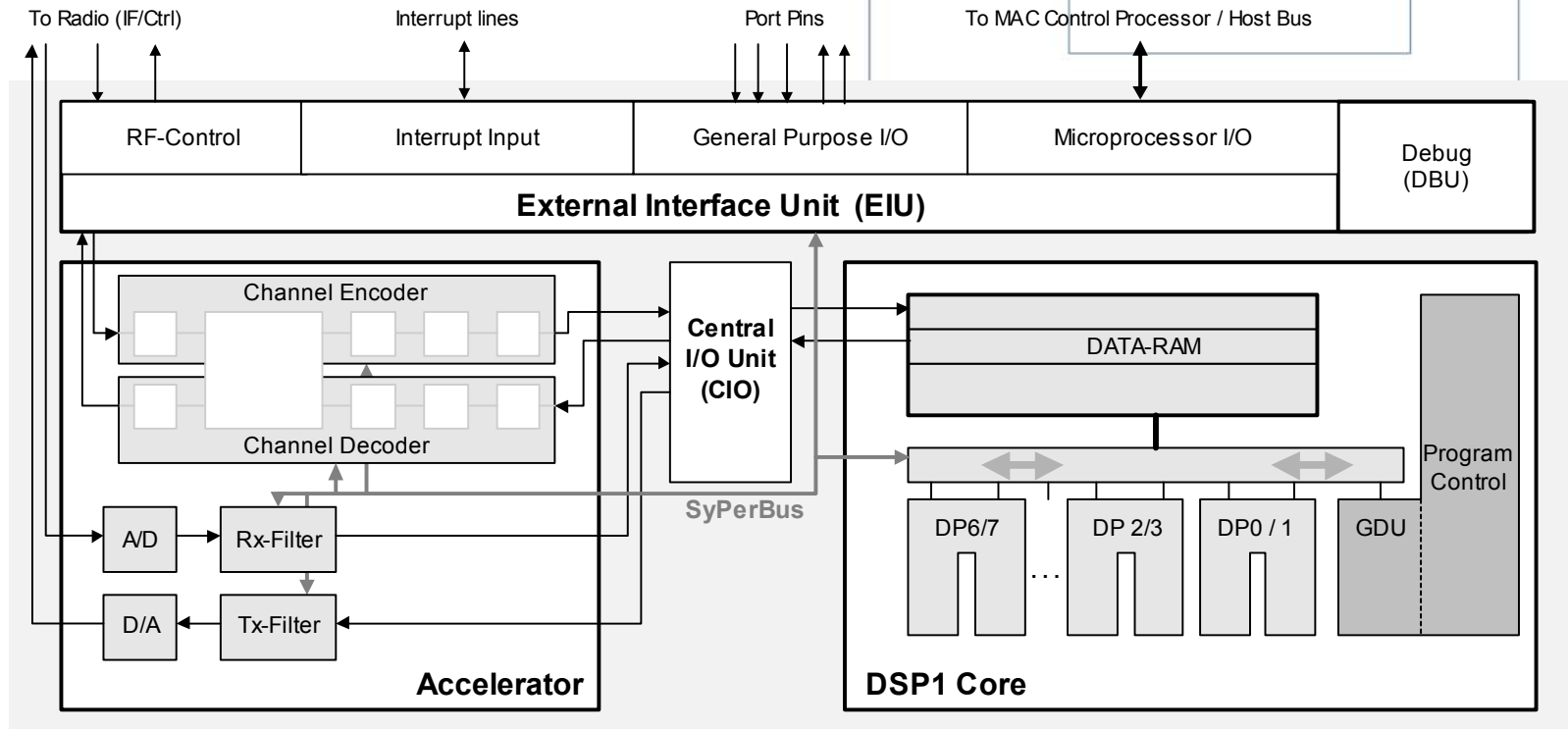
802.11b Signal Acquisition /Preamble Processing



802.11a Signal Acquisition /Preamble Processing



Tondelayo Baseband Block Diagram



802.11a/b/g, HiperLAN/2

Embedded Processor vs. Host Based MAC

Embedded Processor Advantages

- Single software platform (typically Arm7/9 based)
- Can tightly couple the processor to the modem function
- Not dependant on PCI/Cardbus bus performance

Host Based Processor Advantages

- Reduced die size and power dissipation
- Provides more flexibility for access point applications
 - May share processor with access point or other network interface
 - Moves QOS queues off chip to host memory
- Eliminates royalty for embedded processor

Systemonic Chose Host Based MAC

Dual Band (802.11a/b) Challenges

Synthesizer Complexity

- 2.4GHz in addition to 5.x GHz
- 5 MHz Channel Boundaries (5.x GHz)
- 1 MHz Channel Boundaries not aligned with 5MHz (2.4GHz)

Switch / Filter Complexity vs. Addition of 2.4GHz PA & LNA

Separate Antennas vs. Combined 2.4/5.x Antenna

- Complexity of filtering in a combined antenna
- Separate Antennas require extra feed lines, board real estate
- Extra feed lines are an issue in Laptop use
- Additional band select switch losses for combined antenna

Control of Power to PA's and LNA's

Layout and space issues

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